What is claimed is:

1. A method fabricating a semiconductor device comprising:

forming a field oxide film on a semiconductor substrate to form an element isolation region;

forming a side wall film formed of an insulation material on a side wall of a gate electrode which is formed on said semiconductor substrate;

injecting ion injection species into said semiconductor substrate using said gate electrode as a mask, thereby forming a diffusion layer;

activating said diffusion layer by a first thermal treatment;

depositing titanium on the entire surface of said semiconductor substrate and performing a second thermal treatment, thereby forming a Ti silicide either on said gate electrode or on said diffusion layer in a self-aligned manner; and

partially removing the titanium which is not converted to the Ti silicide,

wherein a third thermal treatment at a temperature lower than that of the first thermal treatment for the activation is carried out between the ion injection for forming said diffusion layer and the first thermal treatment for activating said diffusion layer, thereby discharging fluorine produced from the ion injection species to the outside from a surface of said field oxide film, a surface of said side wall film, said semiconductor

substrate, and an interface between said semiconductor substrate and said field oxide film.

2. The method as claimed in claim 1, wherein said third thermal treatment is consecutively performed in the same apparatus as that of said first thermal treatment for activating said diffusion layer.

3. The method as claimed in claim 1, wherein said ion injection species injected into said diffusion layer are ions including fluorine and boron.

4. The method as claimed in claim 1, wherein a fluorine concentration is set to be 1E20 atom/cm^3 or less by said third thermal treatment.

5. The method as claimed in claim 1, wherein a temperature of said third thermal treatment is at a range of 300 to 750 ℃.

6. The method as claimed in claim 1, wherein an apparatus for carrying out said third thermal treatment is a diffusion furnace, a RTP apparatus and a hot plate.

7. A method of fabricating a semiconductor device comprising:

forming an isolation region around a predetermined area of a semiconductor substrate;

selectively forming an insulating layer on said predetermined area;

selectively forming an electrode on said insulating layer;

injecting an impurity ion in said substrate which

is between said electrode and said isolation region;

applying heat of a first temperature to said substrate; and

applying heat of a second temperature higher than said first temperature to said substrate for activating said impurity ion after applying heat of said first temperature.

8. The method as claimed in claim 7, wherein said impurity ion includes fluorine.

9. The method as claimed in claim 8, wherein said applying heat of said first temperature applies said semiconductor device to discharge fluorine included in said isolation region.

10. The method as claimed in claim 7, further comprises selectively forming a siliside on said electrode.

11. The method as claimed in claim 10, wherein said siliside has C49 phase.

12. The method as claimed in claim 11, further comprises changing a phase of said siliside from C49 to C54.

13. The method as claimed in claim 12, wherein said impurity ion includes fluorine.

14. The method as claimed in claim 13, wherein said applying heat of said first temperature applies said semiconductor device to discharge fluorine included in said isolation region.

15. The method as claimed in claim 7, further comprises forming a side wall to a side of said electrode.

16. The method as claimed in claim 15, further comprises selectively forming a siliside on said electrode.

17. The method as claimed in claim 16, wherein said siliside has C49 phase.

18. The method as claimed in claim 17, further comprises changing a phase of said siliside from C49 to C54.

19. The method as claimed in claim 15, wherein said impurity ion includes fluorine.

20. The method as claimed in claim 19, wherein said applying heat of said first temperature applies said semiconductor device to discharge fluorine included in said isolation region and said side wall.

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